between the time the signal at the input pin (terminal 2) of a 2-input AND element goes from low to high (rises) and the time the signal at the output pin (terminal 3) goes from low to high (rises) is 5 ns. Note that delay time information on the rise and fall of input and output pins, such as that shown in FIG. 1(b), is contained also in the conventional delay analysis library."

IN THE CLAIMS:

Please enter the following amended claims:

1. A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library containing connection information on a plurality of circuits and delay time information on rises and falls of each input terminal and output terminal of said plurality of circuits,

wherein said library further contains logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of said plurality of circuits, and

wherein, when making a delay analysis of the logic circuit including at least one of said plurality of circuits, a delay time is selected from said delay time information according to a logic operation of said circuit.

2. A delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library containing connection information on a plurality of circuits and delay time information on rises and falls of each input terminal and output terminal of said plurality of circuits,

wherein said library further contains logical operation information representing correspondence between a logical value of each input terminal and a logical value of the output terminal of at least one of said plurality of circuits, and

wherein, when making a delay analysis of a logic circuit, a delay time between the input terminal and the output terminal is selected from said delay time information according to a logic operation of said circuit,

3. A method for making a delay analysis of a logic circuit, comprising the steps of:

referencing a delay analysis library containing connection information on a plurality of circuits, delay time information on rises and falls of each input terminal and output terminal of at least one of said plurality of circuits, and logic operation information representing correspondence between a logical value of each input terminal and a logical value of the output terminal of at least one of said plurality of circuits; and

selecting the delay time of at least one of said circuits from said delay time information according to a specified logic operation of said circuit.

4. A computer-readable medium having stored thereon a program for executing:

(a) a process step comprising:

referencing a delay analysis library containing connection information on a plurality of circuits, delay time information on rises and falls of each input terminal and output terminal of each one of said plurality of circuits, and logic operation information representing

correspondence between a logical value of each input terminal and a logical value of the output terminal of each one of said plurality of circuits; and

selecting the delay time of at least one of said circuits from said delay time information according to a logic operation of said circuit; and

(b) a process step of performing a delay calculation using said selected delay time as a propagation delay time of said at least one of circuits.